In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

1. (Currently amended) A device that receives and processes signals from a telephone line and supports a plurality of telephone signal protocols, comprising:

a converter circuit that digitizes input signals received on the telephone line, the converter circuit providing a digital signal having components associated with the plurality of telephone signal protocols; and

a digital filter circuit, coupled to the converter circuit to receive the digital signal, the digital filter circuit adapted to convert a sample rate of the digital signal, the digital filter circuit comprising:

a first sample rate converter to convert the sample rate of the digital signal in support of a first of the plurality of the telephone signal protocols to provide a first converted digital signal; and

a second sample rate converter to convert [[wherein the digital filter converts]] the sample rate of the digital signal by an amount that [varies] is capable of being varied during the operation of the device in response to at least one control signal to provide a [[first output]] second converted digital signal having a variable sample rate, the [[first output]] second converted digital signal associated with a [[first]] second of the plurality of telephone signal protocols.

2. (Canceled)

3. (Previously presented) The telephony device of claim 1 wherein the digital filter circuit comprises a first variable-ratio decimation filter.

4. (Canceled)

5. (Previously presented) The telephony device of claim 3 wherein the first variable-ratio decimation filter provides the first output signal, which is associated with a DSL protocol, and wherein the digital filter circuit further comprises a second variable-ratio decimation filter that provides a second output signal, which is associated with a POTS protocol.

6-13. (Canceled)

14. (Currently amended) A device that processes signals to be provided over a communication link in support of a plurality of signal protocols, the device comprising:

a first sample-rate converter that converts a sample rate of a first digital signal associated with a first protocol of the plurality of signal protocols to provide a first converted digital signal, the first sample rate converter converting the sample rate of the first digital signal by an amount that is capable of being varied during operation of the device according to at least one control signal received by the first sample-rate converter;

a second sample-rate converter that converts a sample rate of a second digital signal associated with a second protocol of the plurality of signal protocols to provide a second converted digital signal; and

a digital to analog converter configured to receive a combined digital signal formed from the first converted digital signal and the second converted digital signal and to convert the combined digital signal to a single analog signal associated with both the first protocol and the second protocol.

15. (Canceled)

16. (Currently amended) The device of claim 14 wherein the first sample-rate converter comprises an interpolation filter to receive the first digital signal, the interpolation filter having a variable interpolation ratio capable of being varied according to the control signal to provide the first converted digital signal.

17. (Canceled)

18. (Currently amended) A device that receives and processes signals from a communication link and supports a plurality of signal protocols, comprising:

an analog to digital (A/D) converter, coupled to the communication link, that receives an analog input signal indicative of a signal on the communication link and outputs a digital signal [[sampled data stream]] representative of the analog input signal, the digital signal having components associated with the plurality of signal protocols; and

a digital filter, coupled to the A/D converter, the digital filter comprising:

a first decimation filter that receives the digital signal and converts a sample rate of the digital signal by an amount that is capable of being varied during the operation of the device according to at least one control signal received by the first decimation filter to provide a first sample-rate converted digital signal having a first sample rate, the first sample-rate converted digital signal associated with a first of the plurality of protocols; and

a second decimation filter that receives the digital signal and converts the sample rate of the digital signal to provide a second sample-rate converted digital signal having a second sample rate, the second sample-rate converted digital signal associated with a second of the plurality of protocols.

19-22. (Canceled)

23. (Previously presented) The device of claim 18 wherein the first sample-rate converted digital signal is associated with a POTS signal protocol, and the second sample-rate converted digital signal is associated with a protocol selected from a group consisting of ADSL and IDSN, and a different type than POTS.

24-25 (Canceled).

26. (Previously presented) The device of claim 18, wherein the plurality of signal protocols includes a first signal protocol that occupies a first bandwidth and a second signal protocol that occupies a second bandwidth that does not overlap the first bandwidth.

27-28 (Canceled).

29. (Previously presented) The device of claim 18 wherein the digital filter further comprises at least two interpolation digital filters, each of the at least two interpolation digital filters having an association with a respective one of the first signal protocol and the second signal protocol.

30-36. (Canceled)

37. (Currently amended) The device of claim [[36,]] 1 wherein the second sample rate converter is configured to convert the sample rate of the digital signal by an amount that varies according to operation characteristics of the device.

38. (Canceled)

39. (Currently amended) The device of claim [[38,]] 18 wherein the [[first decimation filter has a variable reduction factor that varies in response to]] at least one control signal is responsive to at least one operating characteristic of the device.

40. (Previously presented) The device of claim 39, wherein the control signal is part of a phase lock loop that includes the first decimation filter.

41. (New) The device of claim 40, wherein the phase lock loop does not include the A/D converter.

42. (New) The device of claim 41, wherein the A/D converter to operates on a fixed-rate clock to provide the digital signal with a fixed sample rate.